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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,366	05/18/2005	Takashi Abe	09792909-6253	7105

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EXAMINER	
HSU, AMY R	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
04/01/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/535,366	ABE ET AL.	
	Examiner	Art Unit	
	AMY HSU	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6 and 21-23* is/are pending in the application.

4a) Of the above claim(s) *3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/17/2009 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1-3, 5, and 6 have been considered but are moot in view of the new ground(s) of rejection. The final rejection (dated 10/17/2008) used the sixth embodiment of Tanaka (US 6674470) in view of the first embodiment of Tanaka to teach that it is well known for the signal wiring in a pixel unit to serve the purpose of light shielding since the wiring metals cover the portion other than the photodiode. The Office maintains this rationale as valid, and does not argue that the drain wiring of Fig. 28C of Tanaka is the full face signal line. However in view of the current amendments, in order to teach more specifically that the full face signal line which selects the pixels is also used as a light shielding function a new reference is cited.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 5-6, 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 6674470) in view of Shaw et al. (US 6606122).

Regarding Claim 1, Tanaka teaches in the first embodiment, a solid-state imaging device comprising:

an imaging area having a plurality of unit cells in a two-dimensional array (*Fig. 3)*, each unit cell of the plurality of unit cells including a group of a predetermined number of pixels (*Fig. 7)*;

a plurality of signal lines to select the pixels (*Fig. 7 reference numbers 38-1 and 40-1, "photodiode selection lines")*, **including a full-face signal line and a reset signal line (*Fig. 7 reference number 38-1 is the full face-signal line which is a pixel selection line and reference number 26-1 is a reset signal line)***, wherein each unit cell includes a plurality of photoelectric converters corresponding to the pixels (*Fig. 7 reference numbers 92a and 92b)*;

an amplifying unit, shared by the pixels, to amplify a signal readout from each photoelectric converter and output an amplified readout signal (*reference number 94, shared by the pixels corresponding to 92a and b photodiodes)*; and

a supply element to supply the readout signal to the amplifying unit (*reference numbers 93a and b are readout transistors to supply the signal from the photodiode to the gate of the amplifying unit, 94)* and

wherein, the signal line used to drive the amplifying unit is the full-face signal line shared by the pixels and driving the full-face signal line allows the signal to be read out from each pixel (*Col 7 Lines 54-55 teaches that the reset transistor 96 charges, or drives, the amplifying transistor 94. Therefore the reset line, reference number 36-1, is the full-face signal line which charges the amplifier allowing the signal to be read out from the pixels. Also this full face signal line is shared by at least pixels corresponding to the photodiodes 92a and b)*.

However, Tanaka does not teach that the full-face signal line serves as a light shielding film and has an opening corresponding to a light receiving surface for every pixel.

It is well known to those of ordinary skill in the art that the signal wiring of the pixel unit is not light sensitive and only the photodiode is, and thus the signal wiring is light shielding if it is above the photodiode. Shaw specifically teaches in Fig. 9 and Col 9 Lines 44-48 that in a pixel unit layout the metal which is used as pixel selection is a metal that is used as a light shield.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Tanaka with that of Shaw to realize that the full face signal line which is a pixel selection line is also a light shielding element. This would have been obvious because any metal in the layer above the light shielding element other than the area above the photodiode for the light path, must be light shielding in order for the light to be received exactly on the photosensitive area for optimal light receiving quality.

Regarding Claim 2, Tanaka teaches the solid-state imaging device according to claim 1, further comprising a reset unit to reset an input section of the amplifying unit (*reference number 96 and Col 7 Lines 54-55)* **when a reset signal is supplied by the reset signal line (*Col 8 Lines 65-67)*.**

Regarding Claim 5, Tanaka teaches the solid-state imaging device according to claim 2, further comprising: a full-face selection signal that passes through the full-face signal line to drive the reset unit and the amplifying unit (*signal line 36-1 drives the reset means which, as it is directly connected to reference number 96, the reset transistor, which in turn resets the amplifying transistor 94)*, wherein, the full-face selection signal is changed from an active state to a non-active state at a time outside a readout operation period of the pixel (*Fig. 8 shows the state of the full face signal line, 36-1, is changed from active to non-active state outside the readout period)*.

Regarding Claim 6, Tanaka teaches the solid-state imaging device according to claim 2, wherein the reset unit is a transistor (*Fig. 7 reference number 96)*, and wherein a full-face selection signal passing through the full-face signal line is changed to an active state during a readout period of the pixel, the reset signal supplied to a gate of the reset unit **through the reset signal line (*Col 8 Lines 65-67)*** is changed to a non-active state, and a driving signal supplied to a transfer unit **through a transfer signal line** is changed to the active state to read out a charge signal stored in the photoelectric converter (*this well known process of reset and readout, transfer and output are illustrated in the timing diagram of Fig. 8)*.

Regarding Claim 21, Tanaka teaches the solid-state image device according to claim 2, wherein the full-face signal line is connected to drains of the reset unit and the amplifying unit. In Fig. 7, the full face signal line, reference number 38-1 is connected to drains of the reset unit and the amplifying unit. Although the full face signal line is directly connected to the gate of the read out transistor, there are signal lines connecting the line to the drains of the reset and amplifying transistors.

Regarding Claim 22, Tanaka teaches the solid-state imaging device according to claim 1, wherein the reset signal line controls a voltage supplied to a gate of a reset unit (*Fig. 7 the reset line reference number 36-1 is connected to the gate of the reset transistor, and Col 8 Lines 65-67)*

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Regarding Claim 23, Tanaka teaches the solid-state image device according to claim 1, but does not teach in the first embodiment at least one transfer signal line to control at least one transfer unit. It is very well known for a pixel unit to have the option of a transfer transistor and transfer line. The sixth embodiment in Fig. 31 and Col 23 Lines 21-25 teaches another embodiment using a transfer transistor and transfer line.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of the first embodiment of Tanaka with that of the sixth embodiment to use a transfer transistor for transferring photoelectric charges from the photodiode to a floating sensing node in a standard four transistor pixel unit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AMY HSU whose telephone number is (571)270-3012. The examiner can normally be reached on M-F 8am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on 571-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amy Hsu
Examiner
Art Unit 2622

/NHAN T TRAN/
Primary Examiner, Art Unit 2622